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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/532,915	03/22/2000	Masahiko Hayakawa	SEL 170	8547

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EXAMINER	
SEFER, AHMED N	

ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 10/30/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/532,915	HAYAKAWA ET AL.	
	Examiner	Art Unit	
	A. Sefer	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 August 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-11 and 14-58* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-11 and 14-58* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 21 .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 8/8/03 has been entered; and new claim 58 has been added.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-3, 5, 6 and 10 are rejected under 35 U.S.C. 102(b) as being anticipated by Iyer et al. (WO 99/10918).

Iyer et al disclose (see figs. 1-3 and page 8) a semiconductor device having a thin film transistor, the semiconductor device comprising a silicon oxide nitride film 106 formed over a substrate 100 or an insulating film formed over a substrate and having at least a silicon oxide nitride film 106 and an insulating layer containing silicon an oxygen 102 (as in claim 3) or made of silicon oxide (as in claim 10); and an active region 120 (see page 8, lines 10-20) formed over the silicon oxide nitride film, wherein the silicon oxide nitride film falls within the claimed

range of 0.3 to 1.6 in a ratio of the concentration of nitrogen to the concentration of silicon; wherein the silicon oxide nitride film falls within the claimed range of 0.1 to 1.7 in a ratio of the concentration of oxygen to the concentration of silicon (as in claim 2).

As to claims 5 and 6, Iyer et al disclose a silicon oxide nitride film 306 in contact with a surface of a substrate.

4. Claims 1-11 and 58 are rejected under 35 U.S.C. 102(b) as being anticipated by Teramoto USPN 5,773,325.

Teramoto disclose (see figs. 1-3, col. 1, lines 32-38, col. 2, lines 47-55 and claim 2) a semiconductor device having a thin film transistor, the semiconductor device comprising a silicon oxide nitride film formed over a substrate 301 or an insulating film formed over a substrate and having at least a silicon oxide nitride film 302 and an insulating layer containing silicon and oxygen 305 (as in claim 3) or made of silicon oxide (as in claims 10 and 11); and an semiconductor film 304 formed over the silicon oxide nitride film or a non-single crystal semiconductor film formed over the silicon oxide nitride film (as in claim 4), wherein the silicon oxide nitride film falls within the claimed range in a ratio of the concentration of nitrogen to the concentration of silicon; wherein the silicon oxide nitride film falls within the claimed range in a ratio of the concentration of oxygen to the concentration of silicon (as in claim 2).

As to claims 5 and 6, Teramoto discloses a silicon oxide nitride film 302 in contact with a surface of a substrate.

As to claims 7 and 8, Teramoto discloses a semiconductor film in contact with a surface of an insulating layer containing silicon and oxygen.

As to claim 9, Teramoto discloses an insulating layer containing silicon and oxygen made of silicon oxide nitride containing silicon, oxygen and nitrogen and wherein a ratio of the concentration of nitrogen to the concentration of silicon falls within the claimed range.

5. Claims 18 and 19 are rejected under 35 U.S.C. 102(b) as being anticipated by Yamazaki et al (JP 9-162405).

Yamazaki et al disclose (see fig. 4, abstract and machine translated version) a semiconductor device comprising an insulating underlying film formed over a substrate 401 and having at least a silicon oxide nitride film 402 and an insulating layer containing silicon and oxygen 406; and a semiconductor film 404 comprising a channel forming region 416 provided over the insulating underlying film; a gate insulating film (upper portion of layer 406) provided over the channel forming region; and a gate electrode 411 provided adjacent to the channel forming region and over the gate insulating film, wherein the silicon oxide nitride film falls within the claimed range in a ratio of the concentration of nitrogen to the concentration of silicon; wherein the silicon oxide nitride film falls within the claimed range in a ratio of the concentration of oxygen to the concentration of silicon (as in claim 19); wherein the silicon oxide nitride film has a thickness that falls within the claimed range of 50-200 nm, and wherein the insulating layer containing silicon and oxygen has a thickness that falls within the claimed range of 10-300 nm.

6. Claims 20 and 21 are rejected under 35 U.S.C. 102(b) as being anticipated by Teramoto

Teramoto disclose (see figs. 1-3, col. 1, lines 32-38, col. 2, lines 47-55 and claim 2) a semiconductor device comprising silicon oxide nitride 205 film over a substrate; a first transistor provided in a pixel and over silicon oxide nitride film; a first semiconductor film comprising a

first channel forming region of said first transistor; a source region 208 and a drain region 206 provided in said first semiconductor film and sandwiching said first channel forming region; a first gate insulating film (upper portion of 205) provided over said first channel forming region; a first gate electrode 206 provided adjacent to said first channel forming region and over said first gate insulating film; a pixel electrode 211provided over a substrate and connected with one of said source region and said drain region; a second transistor provided in a driver and over an silicon oxide nitride film 107; a second semiconductor film comprising a second channel forming region of said second transistor; a second gate insulating film (upper portion of 107) provided over said second channel forming region; a second gate electrode 108/109provided adjacent to said second channel forming region and over said second gate insulating film; wherein the silicon oxide nitride film falls within the claimed range in a ratio of the concentration of nitrogen to the concentration of silicon; wherein the silicon oxide nitride film falls within the claimed range in a ratio of the concentration of oxygen to the concentration of silicon (as in claim 21).

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 4 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Iyer et al.

Iyer et al disclose (see figs. 1-3 and page 8) an insulating film formed over a substrate and having at least a silicon oxide nitride film 106 and an insulating layer containing silicon and oxygen 102 or made of silicon oxide (as in claim 11); and a semiconductor film 120 formed over the silicon oxide nitride film, wherein the silicon oxide nitride film falls within the claimed range of 0.1 to 1.7 in a ratio of the concentration of oxygen to the concentration of silicon.

Iyer et al do not specifically disclose a non-single crystal semiconductor film formed over an insulating layer. However, it would have been obvious to one skilled in the art at the time the invention was made to employ an art-recognized material non-single crystal semiconductor film, since that would provide a high switching speed and a high mobility.

9. Claims 7 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Iyer et al

Iyer et al disclose all the claimed subject matter, but do not teach a semiconductor film in contact with a surface of a silicon oxide layer.

However, it would have been obvious to one skilled in the art at the time the invention was made to modify the invention of Iyer et al such that a semiconductor film is in contact with a surface of a silicon oxide layer, since that would improve the characteristic and reliability of a gate insulating film.

10. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Iyer et al.

Iyer et al disclose all the claimed subject matter including a silicon oxide nitride film that falls within the claimed range of 0.1 to 0.8 in a ratio of the concentration of nitrogen to the concentration of silicon except for another layer of silicon oxide nitride.

It would have been obvious to one skilled in the art at the time the invention was made to employ another silicon oxide layer, since it has been held that mere duplication of the essential

working parts of a device involves only routine skill in the art. St. Regis Paper Co. V. Bemis., 193 USPQ 8.

11. Claims 18 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Iyer et al. in view of Van der Groen et al. US Patent No. 6,093,577.

Iyer et al disclose (see figs. 1-3, pages 8 and 11) an insulating underlying film formed over a substrate and having at least a silicon oxide nitride film 106 and an insulating layer containing silicon and oxygen 102; and a semiconductor film 120 formed over the insulating underlying film, wherein the silicon oxide nitride film falls within the claimed range of 0.3 to 1.6 in a ratio of the concentration of nitrogen to the concentration of silicon; wherein the silicon oxide nitride film falls within the claimed range of 0.1 to 1.7 in a ratio of the concentration of oxygen to the concentration of silicon (as in claim 19); wherein the silicon oxide nitride film has a thickness that falls within the claimed range of 50-200 nm, and wherein the insulating layer containing silicon and oxygen has a thickness that falls within the claimed range of 10-300 nm.

Van der Groen et al disclose (see figs. 1-10 and col. 5, lines 60-65) a semiconductor film comprising a channel forming region provided over an insulating underlying film 13; a gate insulating film provided channel forming region; and a gate electrode provided adjacent to the channel forming region and over the gate insulating film.

Therefore, it would have been obvious to one skilled in the art at the time the invention was made to incorporate the teaching of Van der Groen et al with the invention of Ivery et al, since that would increase the integration of the device.

12. Claims 20, 14-17 and 21-57 are rejected under 35 U.S.C. 103(a) as being unpatentable over Iyer et al. in view of Van der Groen et al. US Patent No. 6,093,577.

Iyer et al disclose (see figs. 1-3, pages 8 and 11) a silicon oxide nitride film 106 over a substrate; wherein the silicon oxide nitride film ranges from 0.3 to 1.6 in a ratio of the concentration of nitrogen to the concentration of silicon; wherein the silicon oxide nitride film falls within the claimed range of 0.1 to 1.7 in a ratio of the concentration of oxygen to the concentration of silicon (as in claim 21).

Van der Groen et al disclose (see figs. 1-10 and col. 5, lines 60-65) a film transistor provided in a pixel and over silicon oxide nitride film 13; a first semiconductor film comprising a first channel forming region of said first transistor; a source region and a drain region provided in said first semiconductor film and sandwiching said first channel forming region; a first gate insulating film provided over said first channel forming region; a first gate electrode provided adjacent to said first channel forming region and over said first gate insulating film; a pixel electrode 8 provided over a substrate and connected with one of said source region and said drain region; a second transistor provided in a driver and over said silicon oxide nitride film; a second semiconductor film comprising a second channel forming region of said second transistor; a second gate insulating film provided over said second channel forming region; a second gate electrode provided adjacent to said second channel forming region and over said second gate insulating film.

Therefore, it would have been obvious to one skilled in the art at the time the invention was made to incorporate the teaching of Van der Groen et al with the invention of Ivery et al, since that would increase the integration of the device.

As to claims 14-17 and 22-57, the prior art omits that electronic equipment selected from the group consisting of a video camera, a digital camera and other various electronic equipment.

However, Examiner takes Official Notice that an electronic equipment comprising a display device wherein said electronic equipment selected from the group consisting of a video camera or a digital camera is conventional and well known. Therefore, it would have been obvious to one skilled in the art at the time the invention was made to have used any of the various electronic equipment since Examiner takes Official Notice that due to their low power consumption, displays have become a necessary and indispensable structural element of an electronic equipment.

Conclusion

13. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Aronowitz et al. USPN 6,087,229 disclose a composite semiconductor gate dielectrics.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to A. Sefer whose telephone number is (703) 605-1227.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on (703) 308-6601.

ANS
October 22, 2003

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